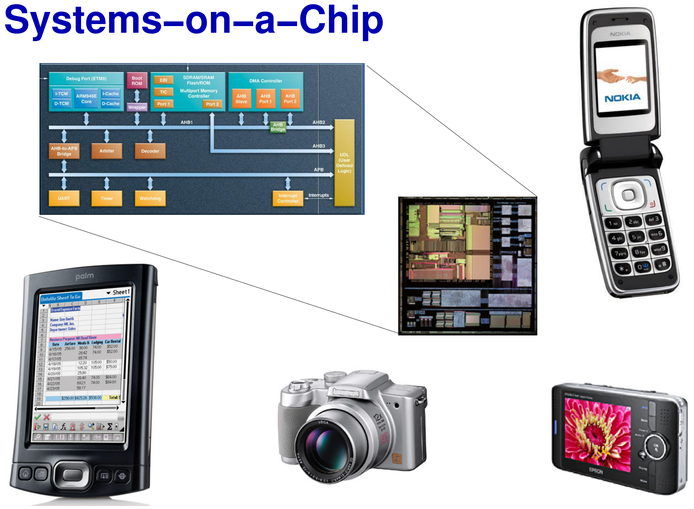
Validation of Systems–on–a–Chip at the Transactional Level

STMicroelectronics/UJF–VERIMAG Common Lab

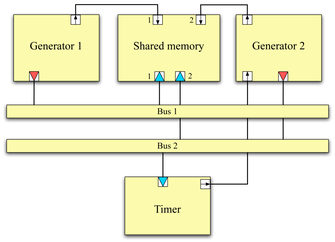
openTLM : a Minalogic project

UJF–VERIMAG / Synchrone
STMicroelectronics HPC / SPG Group

Systems–on–a–Chip



C++/SystemC: a Standard for TLM Design



A SystemC program contains:

– The architecture of the SoC
– The embedded software
– The description of the hardware elements

```
SC_MODULE(top)
{
  // Channel
  tac_router<int, int> * BUS;

  // Memories
  tac_memory<int, int> * MEMORY;

  // Timer
  tac_simple_timer * TIMER;

  // Traffic generators
  traffic_generator1 * GENERATOR1;
  traffic_generator2 * GENERATOR2;

 public:
    SC_CTOR(top)
    {
      // Memory instantiation
      MEMORY = new tac_memory<int, int>("MEMORY", 0x4000);

      // Timer instantiation
      TIMER = new tac_simple_timer("TIMER", 10, SC_US);

      // Traffic generator
      GENERATOR1 = new traffic_generator1("GENERATOR1", 0x0);
      GENERATOR2 = new traffic_generator2("GENERATOR2", 0x4000);

      BUS = new tac_router<int,int>("ROUTER");

      // Binding
      BUS->initiator_port(MEMORY->target_port);
      BUS->initiator_port(TIMER->target_port);
      GENERATOR1->initiator_port(BUS->target_port);
      GENERATOR2->initiator_port(BUS->target_port);
      TIMER->int_timer(GENERATOR2->int_timer);
      ...
    }
  ...
};
```

The SystemC Simulation Tool:
– A Non–Preemptive Scheduler

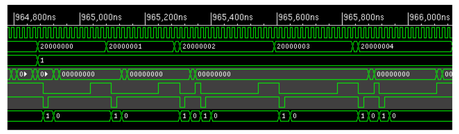
Transaction–Level Modeling for the Development of Systems–on–a–Chip

Transaction Level Models (TLM)
– Pure Functional Models
(PV : Programmer's View)
– Performance Evaluation Models
(PVT : Programmer's View + Time)

+ Fast Simulations
+ Early Availability
– Not Synthesizable
+ Very Abstract
+ Component–Based
+ Allow Early Development of the Embedded Software

No automatic transformations

Synthesizable +
Very Detailed (data and cycle–accurate) +/–
Late Availability –
Slow Simulations –



Register Transfer level Models (RTL)

Challenges:

– Validation of Functional Properties at the TLM Level (test, formal verification)

– Estimation of Non–Functional Properties at the TLM Level (Time, Energy, ...)

– Formal Comparison Between levels of Abstraction

– Design methodologies for Refining Models (PVT from PV, ...)

VERIMAG/ST Joint Work